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(2013.01); *H01L* 2924/00014 (2013.01); *H01L*  
2924/014 (2013.01); *H01L* 2924/0105  
(2013.01); *H01L* 2924/01015 (2013.01); *H01L*  
2924/01029 (2013.01); *H01L* 2924/01033  
(2013.01); *H01L* 2924/01047 (2013.01); *H01L*
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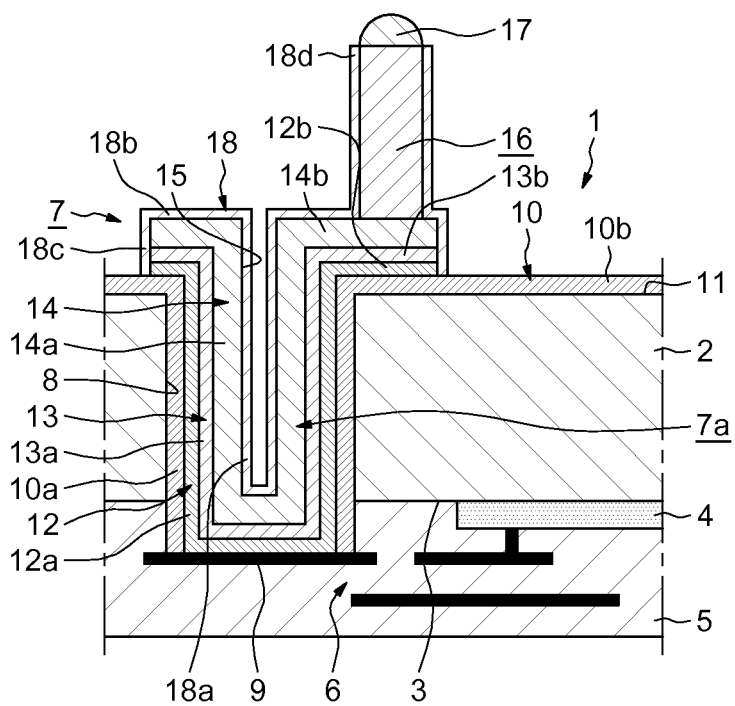


FIG.2

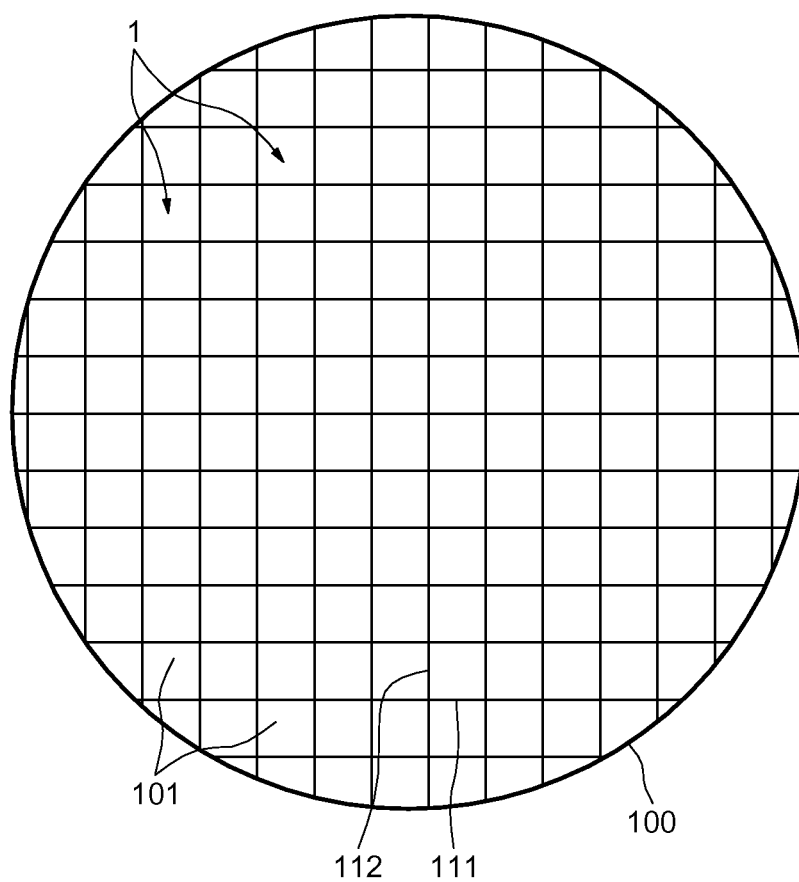


FIG.3

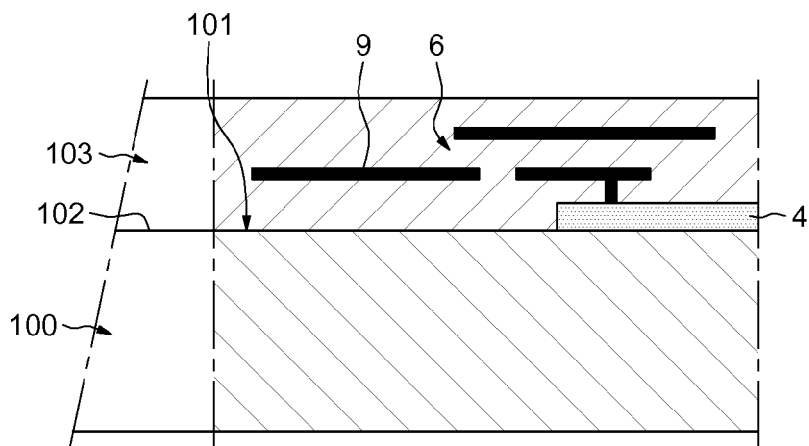


FIG.4

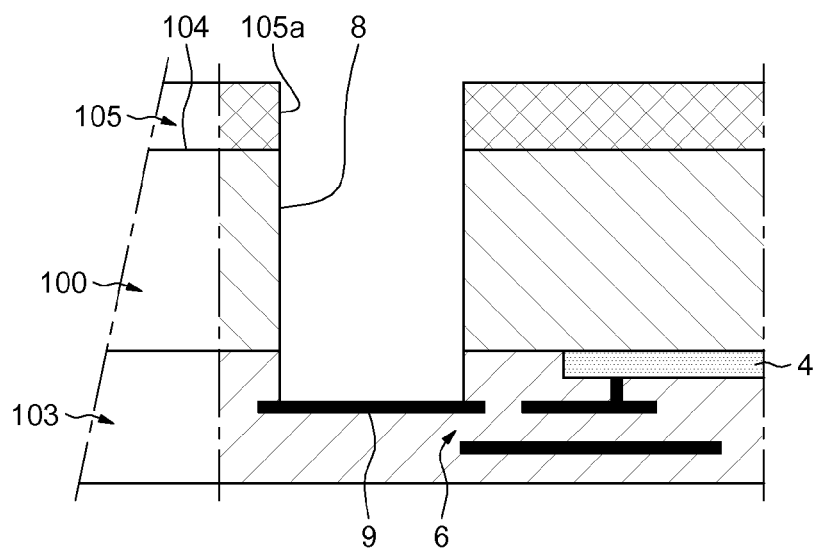


FIG.5

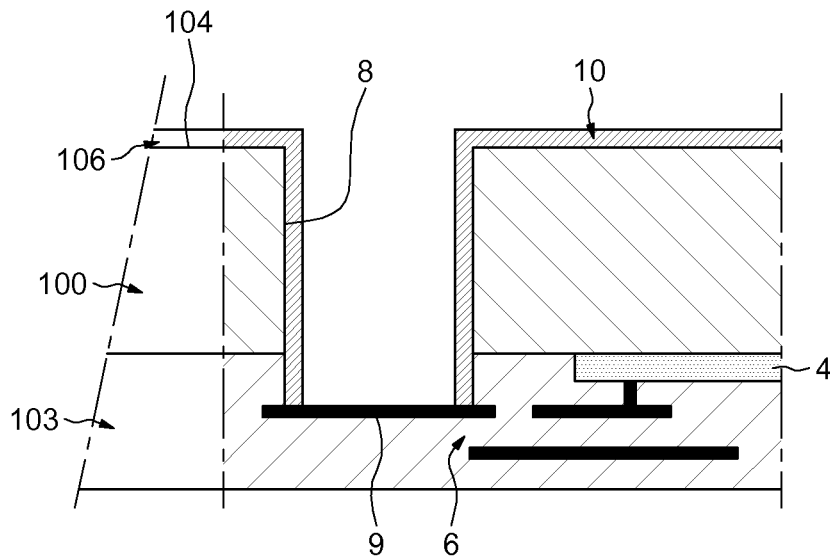


FIG.6

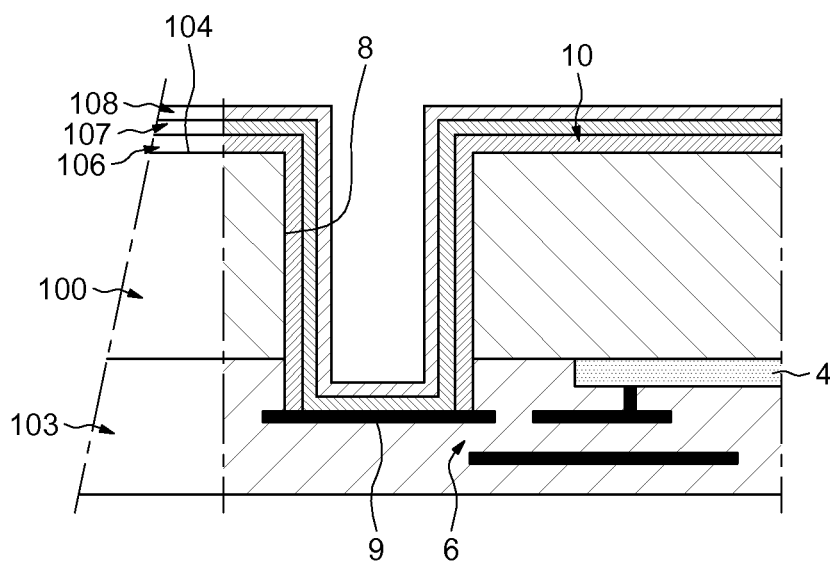


FIG.7

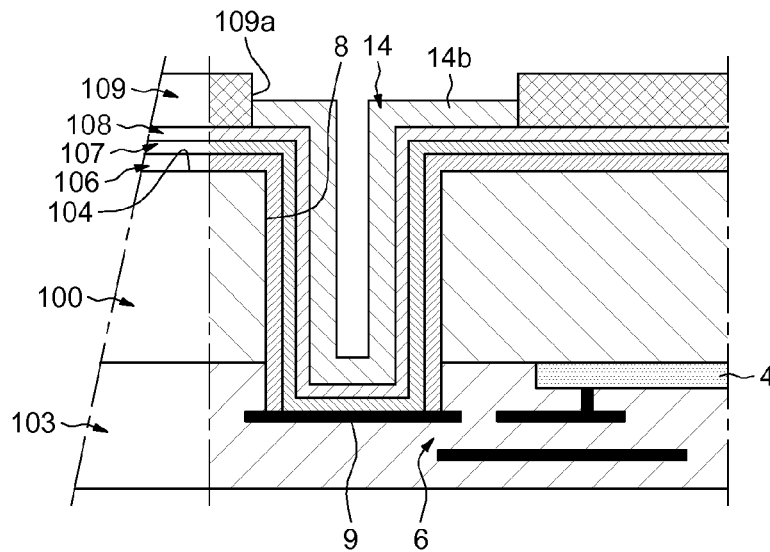


FIG.8

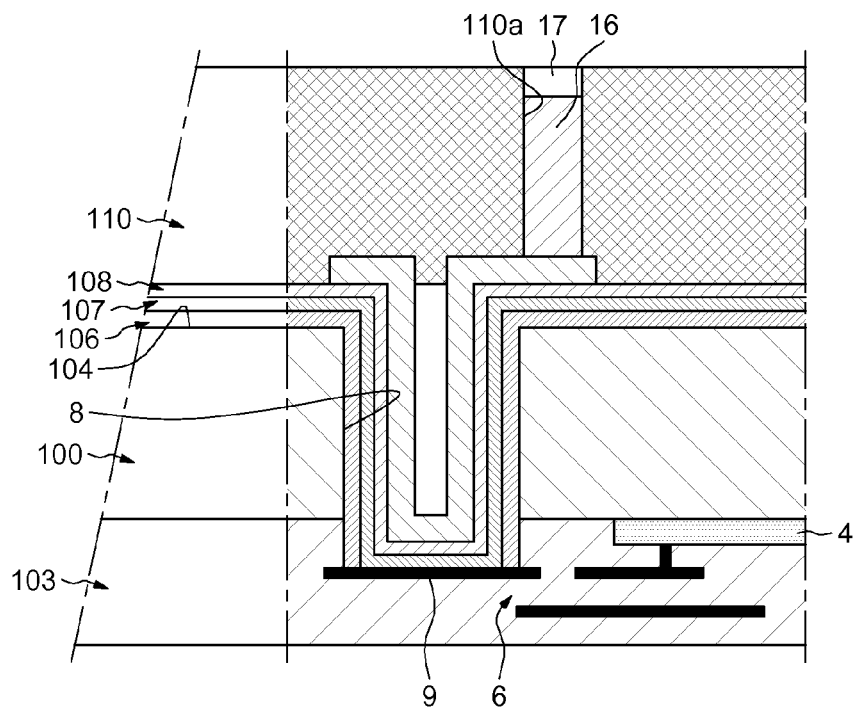


FIG.9

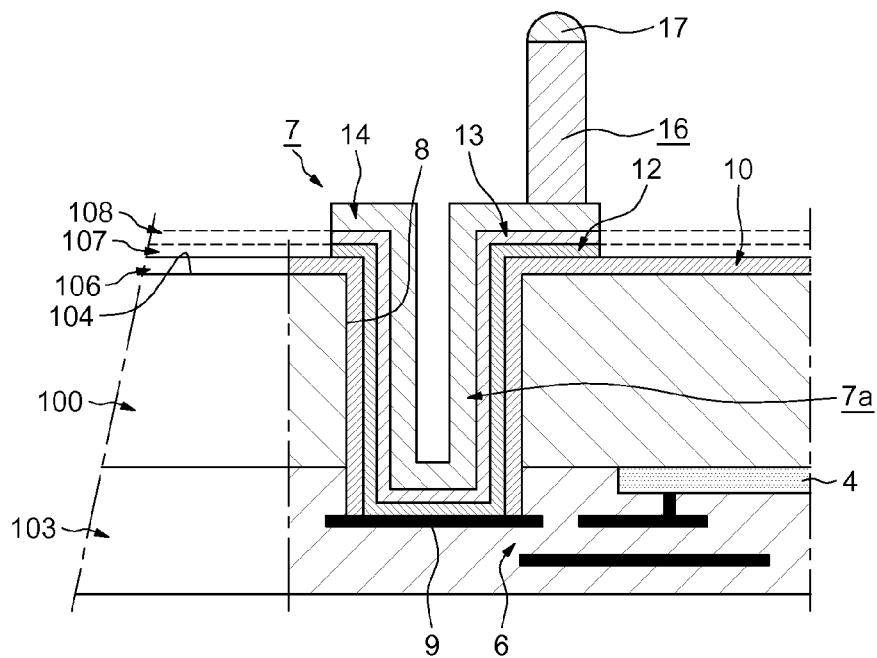
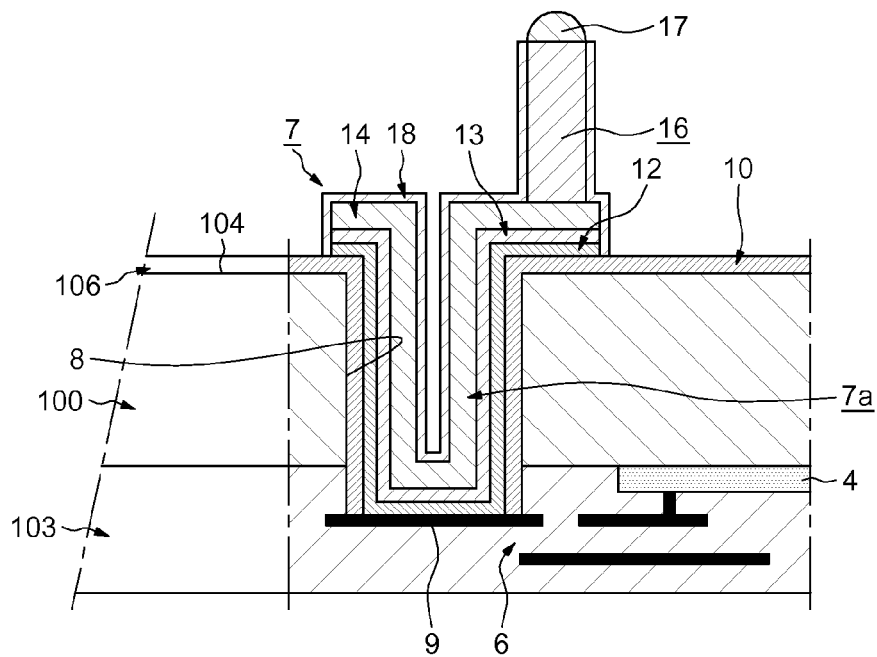


FIG.10





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# INTEGRATED CIRCUIT CHIP AND FABRICATION METHOD

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional from United States Application for patent Ser. No. 13/304,823 filed Nov. 28, 2011, which claims priority from French Application for Patent No. 1061355 filed Dec. 30, 2010, the disclosures of which are hereby incorporated by reference.

## TECHNICAL FIELD

The present invention relates to the field of semiconductor devices and, more particularly, that of integrated circuit chips and their fabrication methods.

## BACKGROUND

Integrated circuit chips are known which are provided with electrical connection means which comprise electrical connection vias for passing through the substrate on a front face of which are formed the integrated circuits, in order to produce electrical connections at the rear, that is to say, opposite the side where the integrated circuits are situated, these electrical connection vias being provided with rear electrical connection pillars. The rear face of the substrate and the vias are covered with a permanent passivation layer made of a photosensitive polymer, through which the rear electrical connection pillars are formed by using non-permanent conductive layers on this passivation layer. Consequently, the fabrication methods implemented comprise a large number of steps in particular because of the existence of the passivation layer. Furthermore, the passivation layer cannot completely fill the central hole remaining in the vias even though there is a risk of internal oxidation of the electrical connection vias.

## SUMMARY

According to one implementation, a fabrication method is proposed that at least partly avoids the abovementioned drawbacks.

A method for producing an electrical connection means of an integrated circuit chip is proposed that comprises a substrate die and, on a front face of the substrate die, integrated circuits and a layer incorporating a front electrical interconnect network.

The proposed method may comprise: producing at least one local electrical connection via made of an electrically conductive material, passing through the substrate die and linked to a connection portion of said electrical interconnect network; producing an electrical connection pillar made of an electrically conductive material, on a rear portion of the electrical connection via; and producing an external local protection layer at least partly covering the electrical connection via and the electrical connection pillar.

The proposed method may comprise: producing a hole through the substrate die via its rear face, revealing a connection portion of said electrical interconnect network; producing, by a physical vapor phase deposition (PVD), a thin layer made of an electrically conductive material, above the rear face of the substrate die and the wall and the bottom of the hole; producing, by a local electrochemical deposition with electrical contact on said thin layer, a local thick layer made of an electrically conductive material on the thin layer,

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in the hole and above the rear face of the substrate die; producing, by a local electrochemical deposition with electrical contact on said thin layer, a rear electrical connection pillar on the thick layer; and removing the thin layer around the thick layer, the remaining portion of the thin layer and the thick layer forming an electrical connection via linked to said front interconnect network and provided with the rear electrical connection pillar.

The method may comprise: producing, by a chemical deposition, an external local protection layer at least partly covering the electrical connection via and the rear electrical connection pillar.

The method may comprise, before producing the thin layer: producing an insulating layer on the rear face of the substrate die and against the walls of the hole; and removing a part of the insulating layer situated above said connection portion of the front electrical interconnect network.

The method may comprise: producing the insulating layer by a sub-atmospheric chemical vapor phase deposition (SACVD).

According to one embodiment, there is proposed an integrated circuit chip comprising a substrate die and, on a front face of this substrate die, integrated circuits and a layer incorporating a front electrical interconnect network.

A proposed integrated circuit chip may comprise at least one rear electrical connection means comprising an electrical connection via passing through the substrate die and linked to a connection portion of said front electrical interconnect network and comprising a rear electrical connection pillar formed on the electrical connection via, and a local rear protection layer at least partly covering the electrical connection via and the electrical connection pillar.

The electrical connection pillar may be provided, on its end, with a drop of solder.

The electrical connection via and the electrical connection pillar may comprise copper (Cu) and the protection layer comprises an alloy of cobalt (Co), tungsten (W) and phosphorus (P).

## BRIEF DESCRIPTION OF THE DRAWINGS

An integrated circuit chip and an integrated circuit chip fabrication method, according to a particular embodiment of the present invention, will now be described as non-limiting examples, illustrated in the drawing in which:

FIG. 1 represents a partial cross-section of an integrated circuit chip;

FIG. 2 represents a wafer of integrated circuit chips; and

FIGS. 3 to 10 represent steps in fabricating integrated circuit chips, seen in cross section.

## DETAILED DESCRIPTION OF THE DRAWINGS

As illustrated in FIG. 1, an integrated circuit chip 1 comprises a substrate die 2, for example made of silicon, on a front face 3 of which are produced integrated circuits 4 and which is provided, on this front face 3, with a front layer 5 in which is incorporated a front electrical interconnect network 6, possibly with several metallic levels, selectively linked to the integrated circuits 4.

The integrated circuit chip 1 comprises a plurality of rear electrical connection means 7, each of which has the following structure.

Through the substrate die 2, and in a region free of integrated circuits 4, a hole 8 is formed which is prolonged (extended) in the front layer 5 to an electrical connection

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portion 9 of the front interconnect network 6. This connection portion 9 may be situated in the first metallic level of the front interconnect network 6.

An insulating layer 10, for example made of silicon oxide ( $\text{SiO}_2$ ), has a part 10a which covers the lateral wall of the hole 8 and a part 10b which covers the rear face 11 of the substrate die 2.

A local electrically conductive barrier layer 12, for example made of titanium (Ti), in a bilayer of titanium nitride and titanium (TiN/Ti), of tantalum (Ta) or of a bilayer of tantalum nitride and tantalum (TaN/Ta), has a part 12a which covers the part 10a of the insulating layer 10 and the connection portion 9, in the bottom of the hole 8, and has a local part 12b which locally covers the part 10b of the insulating layer 10, over at least a part of the periphery of the hole 8.

A local electrically conductive attach layer 13, for example made of copper (Cu), has a part 13a which covers the part 12a of the barrier layer 12 and a local part 13b which covers the local part 12b of the barrier layer 12.

A thick local electrically conductive layer 14, for example made of copper (Cu), has a part 14a which covers the part 13a of the attach layer 13 and a local part 14b which covers the local part 13b of the attach layer 13. The part 14a of the thick layer 14 determines a remaining central blind hole 15 which is open towards the rear. According to a variant embodiment, the thickness of the local thick layer 14 may be sufficient to completely fill the rest of the hole 8 and thus eliminate the central blind hole 15.

An electrically conductive pillar 16, protruding towards the rear, for example made of copper (Cu) is formed on the local part 14b of the thick layer 14, this pillar being, for example, cylindrical.

On the end of the protruding pillar 16, a drop of electrically conductive solder 17 is formed, which is, for example, made of an alloy of tin and silver (SnAg) or an alloy of tin, silver and copper (SnAgCu).

Finally, a local external rear protection layer 18, for example made of an alloy of cobalt, tungsten and phosphorus (CoWP), comprises a part 18a which covers the part 14a of the thick layer 14, in the remaining hole 15, comprises a part 18b which covers the local part 14b of the thick layer 14, around the protruding pillar 16, comprises a part 18c which covers the flanks or lateral edges of the local part 14b of the thick layer 14, of the local part 13b of the layer 13 and of the local part 12, as far as the part 10b of the insulating layer 10, and comprises a part 18d which covers the peripheral face of the protruding pillar 16 and, possibly, the drop of solder 17.

Thus, each rear electrical connection means 7 comprises an electrical connection via 7a formed by the layers 12, 13 and 14 and comprises the protruding pillar 16, the end of which can be soldered to another electronic component via the drop of solder 17, this via 7a and this pillar 16 being protected against corrosion by virtue of the existence of the external protection layer 18.

With reference to FIGS. 2 to 10, there now follows a description of a method for collectively fabricating a plurality of integrated circuit chips corresponding to the integrated circuit chip 1 of FIG. 1.

As illustrated in FIG. 2, there is, for this, a wafer 100, for example made of silicon, having a plurality or matrix of placements 101 each corresponding to an integrated circuit chip 1 to be fabricated.

As illustrated in FIG. 3, integrated circuits 4 and front electrical connection network 6 are produced in a common

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front layer 103, on a front face 102 of the wafer 100 and respectively in the placements 101.

Next, as illustrated in FIG. 4, pluralities of holes 8 are produced, via the rear face 104 of the wafer 100 and respectively in the placements 101 of the chips to be fabricated, by etching through corresponding through passages 105a formed in a mask 105, and as far as portions 9 of the electrical connection networks. Then, the mask 105 is removed.

Next, as illustrated in FIG. 5, using a sub-atmospheric chemical vapor phase deposition (SACVD), an insulating layer 106 is produced on the rear face 104 and in the holes 8 of the wafer 100, and the parts of this layer 106 in the bottom of the holes 8 are removed so as to reveal the portions 9 of the front electrical connection network 6. The insulating layer 10 is thus obtained, in each of the placements 101 and for each chip to be fabricated.

According to a variant embodiment, it would be possible to produce the holes 8 close to the portions 9 of the electrical connection networks 6, in the layer 103, then deposit the insulating layer 106, then remove the parts of this layer 106 in the bottom of the holes 8 and remove the rest of the layer 103 to reveal the portions 9 of the front electrical connection networks 6.

Next, as illustrated in FIG. 6, a layer 107 is produced by a physical vapor phase deposition (PVD), on the insulating layer 106 and in the bottom of the holes 8, followed by a layer 108 on this layer 107, both intended for the fabrication of the layer 12 then the layer 13 of the chips to be fabricated.

Next, as illustrated in FIG. 7, a mask 109 is formed on the layer 108, through which are formed openings 109a, the edges of which correspond to the edges of the rear parts 14b of the local layers 14 associated with the holes 8 of the chips to be fabricated. Then, an electrochemical deposition in a bath is used to produce the local layers 14 in the openings 109a of the mask 109, by making electrical contact on the peripheral edge of the layer 108, at the periphery of the wafer 100.

Next, as illustrated in FIG. 8, after having removed the mask 109, a new mask 110 is formed on the layer 108 and on the local layers 14, by forming, through this mask 110, through openings 110a corresponding to the pillars 16 to be produced on the rear parts 14b of the local layers 14 produced. Then, an electrochemical deposition in a bath is used to produce the pillars 16 and then the drops of solder 17 in the openings 110a of the mask 110, by making, as previously, electrical contact on the peripheral edge of the layer 108, at the periphery of the wafer 100.

Next, as illustrated in FIG. 9, after having removed the mask 110, a wet etch in suitable baths is used to remove the parts of the layer 108 then the previous layer 107, around the rear parts 14b of the local layers 14 produced, over all the remaining surface of the insulating layer 106. Local layers 12, 13 and 14 are then obtained which are associated with each of the holes 8 of the chips to be produced.

Then, a bake is performed for the drops of solder 17 to assume the dome shape.

Thus, pluralities of local rear electrical connection means 7 are formed, in the placements 101 of the wafer 100, each comprising an electrical connection through via 7a and a protruding pillar 16 provided with a drop of solder 17.

Next, as illustrated in FIG. 10, a naturally selective chemical deposition is used to produce protection layers 18 on the rear electrical connection means 7. For example, if the thick layer 14 and the protruding pillar 16 are made of copper, the protection layer 18 may be formed by a selective chemical deposition of a ternary alloy based on cobalt,

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tungsten and phosphorus (CoWP) according to a self-catalytic vapor phase growth method.

Next, as illustrated in FIG. 2, the integrated circuit chips 1 obtained in the placements 101 are singularized, for example by sawing along lines 111 and columns 112 separating these placements 101.

The present invention is not limited to the examples described above. Many other variant embodiments are possible, without departing from the framework defined by the appended claims.

What is claimed is:

1. An integrated circuit chip, comprising:
  - a substrate die;
  - integrated circuits and a layer incorporating a front electrical interconnect network on a front face of the substrate die;
  - at least one rear electrical connection structure comprising:
    - an electrical connection via passing through the substrate die and linked to a connection portion of said front electrical interconnect network;
    - a rear electrical connection pillar formed on the electrical connection via;
    - a local rear protection layer at least partly covering the electrical connection via and the electrical connection pillar; and
    - wherein the electrical connection via and the rear electrical connection pillar are formed of a same metal material.
2. The chip according to claim 1, wherein the same metal material comprises copper (Cu) and the protection layer comprises an alloy of cobalt (Co), tungsten (W) and phosphorus (P).
3. The chip according to claim 1, wherein the rear electrical connection pillar is provided, on its end, with a drop of solder.
4. The chip according to claim 1, wherein the electrical connection via includes a portion on a back face of the substrate die which is offset from a hole in which the electrical connection via is formed, said rear electrical connection pillar formed on said portion of the conductive via located on said back face of the substrate die which is offset from said hole, said rear electrical connection pillar extending perpendicular to said back face of the substrate die.
5. The chip according to claim 1, wherein the rear electrical connection pillar is in the shape of a solid cylinder.
6. An integrated circuit chip, comprising:
  - a substrate die;
  - integrated circuits and a layer incorporating a front electrical interconnect network on a front face of the substrate die;
  - a conductive via extending from a back face of the substrate die to make electrical contact with the front electrical interconnect network, said conductive via including a metal material within a hole and further including a portion of said metal material extending from said hole onto said back face of the substrate die which is offset from said hole in which the conductive via is formed;
  - a rear electrical connection pillar formed on and directly contacting said portion of said metal material located on said back face of the substrate die which is offset

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from said hole, said rear electrical connection pillar extending perpendicular to said back face of the substrate die; and

- a protection layer which at least partly covers the rear electrical connection pillar and said portion of said metal material located on said back face of the substrate die which is offset from said hole.
7. The chip according to claim 6, wherein the metal material of the electrical connection via and the rear electrical connection pillar comprise copper (Cu) and the protection layer comprises an alloy of cobalt (Co), tungsten (W) and phosphorus (P).
8. The chip according to claim 6, wherein the rear electrical connection pillar is provided, on its end, with a drop of solder.
9. The chip according to claim 6, wherein the rear electrical connection pillar is in the shape of a solid cylinder.
10. An integrated circuit chip, comprising:
  - a substrate die having a front face with integrated circuits and a rear face;
  - a layer on the front face incorporating a front electrical interconnect network;
  - a hole in the rear face which extends through the substrate die to a surface of a connection portion of the front electrical interconnect network;
  - an insulation layer covering the rear face of the substrate die and sidewalls of the hole;
  - a local electrical connection via in said hole made of an electrically conductive material that passes through the substrate die and is linked to said connection portion;
  - an electrical connection pillar made of the same electrically conductive material as the local electrical connection via and located on a rear portion of the local electrical connection via; and
  - an external local protection layer at least partly covering the local electrical connection via and the electrical connection pillar.
11. The chip according to claim 10, wherein said same electrically conductive material is copper and the protection layer is an alloy of cobalt (Co), tungsten (W) and phosphorus (P).
12. The chip according to claim 10, wherein the electrical connection pillar is in the shape of a solid cylinder.
13. The chip according to claim 1, wherein the rear electrical connection pillar directly contacts a metal material of the electrical connection via which at least partly fills a hole in the substrate die within which the electrical connection via is formed.
14. The chip according to claim 1, wherein the same metal material comprises copper (Cu).
15. The chip according to claim 6, wherein the rear electrical connection pillar and the conductive via are formed of the same metal material.
16. The chip according to claim 6, wherein the metal material of the electrical connection via and a metal material of the rear electrical connection pillar comprise copper (Cu).
17. The chip according to claim 10, wherein the electrical connection pillar directly contacts a metal material of the local electrical connection via which at least partly fills a hole in the substrate die within which the local electrical connection via is formed.
18. The chip according to claim 10, wherein said same electrically conductive material is copper.

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